AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

Claims 1-12 (canceled)

13. (New) A method of manufacturing a semiconductor device, comprising:

forming source/drain regions in a surface of a semiconductor substrate;

forming a gate insulating film on a surface of the substrate between the source/drain regions; and

forming a gate electrode on the gate insulating film, the gate electrode being set to have a film stress of 200 MPa or less in terms of absolute value, such that a total charge amount is 25 C/cm^2 or more, the total charge amount being an amount of electric charge passing through the gate insulating film when intrinsic dielectric breakdown of the gate insulating film takes place.

14. (New) The method according to claim 13, wherein the gate electrode comprises a polysilicon film doped with an impurity.

15. (New) The method according to claim 14, wherein the gate electrode consists essentially of the polysilicon film.

16. (New) The method according to claim 14, wherein the film stress is a compressive stress.

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17. (New) The method according to claim 13, wherein the gate insulating film comprises a silicon oxide film.

18. (New) The method according to claim 17, wherein the gate insulating film consists essentially of the silicon oxide film.

19. (New) The method according to claim 18, wherein the gate insulating film has a property such that the total charge amount is 25 C/cm^2 or more when the gate insulating film has a thickness of 8 nm and is supplied with an electric field of 12 MV/cm.

20. (New) The method according to claim 14, wherein the polysilicon film is formed by means of a CVD process performed at a film formation temperature of 640°C or more.

21. (New) The method according to claim 20, wherein the film formation temperature is 650°C or more.

22. (New) The method according to claim 20, wherein the semiconductor substrate is rotated at a rotational speed of 3000 rpm or more during the CVD process.

23. (New) A method of manufacturing a non-volatile semiconductor memory device, comprising:

forming source/drain regions in a surface of a semiconductor substrate;

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forming a first gate insulating film on a surface of the substrate between the source/drain regions;

forming a floating gate electrode on the first gate insulating film, the floating gate electrode being set to have a film stress of 200 MPa or less in terms of absolute value, such that a total charge amount is 25 C/cm^2 or more, the total charge amount being an amount of electric charge passing through the first gate insulating film when intrinsic dielectric breakdown of the first gate insulating film takes place;

forming a second gate insulating film on the floating gate electrode; and

forming a control gate electrode on the second gate insulating film.

24. (New) The method according to claim 23, wherein the floating gate electrode comprises a polysilicon film doped with an impurity.

25. (New) The method according to claim 24, wherein the floating gate electrode consists essentially of the polysilicon film.

26. (New) The method according to claim 24, wherein the film stress is a compressive stress.

27. (New) The method according to claim 23, wherein the first gate insulating film comprises a silicon oxide film.

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28. (New) The method according to claim 27, wherein the first gate insulating film consists essentially of the silicon oxide film.

29. (New) The method according to claim 28, wherein the first gate insulating film has a property such that the total charge amount is 25 C/cm^2 or more where the first gate insulating film has a thickness of 8 nm and is supplied with an electric field of 12 MV/cm.

30. (New) The method according to claim 24, wherein the polysilicon film is formed by means of a CVD process performed at a film formation temperature of 640°C or more.

31. (New) The method according to claim 30, wherein the film formation temperature is 650°C or more.

32. (New) The method according to claim 30, wherein the semiconductor substrate is rotated at a rotational speed of 3000 rpm or more during the CVD process.

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